REMARKS

Claims 1-4, 7-11 and 14-22 are pending in the present application. Claims 1, 7-10, 14-16 and 18 have been amended.

Telephone Interview

Applicant respectfully acknowledges the courtesy extended by Examiner Andujar during the telephone interview conducted on November 3, 2006. It is Applicant's understanding that during the telephone interview, the Examiner confirmed that silicon dioxide layer 15 and photoresist layer 16 in Fig. 4 of Japanese Patent Publication No. 2000-133572 (hereinafter referred to as the Sony reference) have been interpreted together as the oxidation prevention cover film of the claims. The Examiner asserted that layers 15 and 16 in Fig. 4 of the Sony reference have raised bumps over aluminum Rhine pattern 12, and that the bumps are in the shape of the pattern of Rhine patterns 12 shown in Fig. 3. The Examiner thus asserted that the Sony reference broadly reads on claim 1 pending as of August 31, 2006.

The Examiner also apparently took the position that Rhine patterns 13 in photoresist 16 of Fig. 4 of the Sony reference may be broadly considered as having first through fourth sub-patterns. The Examiner thus asserted that the Sony reference broadly reads on claim 9 of the present application. Regarding claim 16, the Examiner questioned the scope and meaning of "annular", and thus subsequently asserted that the Sony reference may broadly be considered as meeting the features of claim 16 as

best understood.

Claim Rejections-35 U.S.C. 102

Claims 1, 2, 9, and 16-18 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Sony reference (Japanese Patent Publication No. 2000-133572). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a substrate; an alignment mark "which is formed on the main surface and which has a pattern, wherein the pattern in a plane view has a shape that is obtained by eliminating corners from a polygon"; and strips of oxidation prevention cover film "that are respectively aligned above the alignment mask, that are separated from each other, and that are disposed in the shape of the pattern". Applicant respectfully submits that the Sony reference as relied upon by the Examiner does not disclose these features.

As noted above, the Examiner has interpreted silicon dioxide layer 15 and photoresist layer 16 in Fig. 4 of the Sony reference as an oxidation prevention cover film. However, it would appear in view of Fig. 4 of the Sony reference that silicon dioxide layer 15 and photoresist layer 16 are planar and formed over the entirety of the structure as illustrated, and thus are not strips of oxidation prevention cover film as would be necessary to meet the features of claim 1. Moreover, since silicon dioxide layer 15 and photoresist layer 16 appear to be formed over the entirety of the structure,

silicon dioxide layer 15 and photoresist layer 16 taken together cannot be interpreted as strips of oxidation prevention cover film that are aligned above an alignment mark and that are separated from each other. Also, silicon dioxide layer 15 and photoresist layer 16 in Fig. 4 of the Sony reference do not appear to be disposed in the shape of a pattern obtained by eliminating corners from a polygon, as would be necessary to meet the further features of claim 1. Applicant therefore respectfully submits that the semiconductor device of claim 1 distinguishes over the Sony reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1 and 2, is improper for at least these reasons.

The semiconductor device of claim 9 includes in combination a substrate; an alignment mark "which is formed on the main surface and which has first through fourth mark portions, wherein the first through fourth mark portions are arranged in a pattern so that the first and second mark portions oppose each other, the third and fourth mark portions oppose each other, and the first through fourth mark portions are separated from one another"; and first through fourth sections of oxidation prevention cover film "respectively formed as separated from each other and aligned directly above the first through fourth mark portions in the pattern". Applicant respectfully submits that the relied upon prior art does not disclose these features.

As noted above, the Examiner has interpreted silicon dioxide layer 15 and photoresist layer 16 in Fig. 4 of the Sony reference taken together as an oxidation prevention cover film. However, since layers 15 and 16 in Fig. 4 of the Sony reference

are respectively planar layers that appear to cover the entirety of the structure as illustrated, silicon dioxide layer 15 and photoresist layer 16 cannot be interpreted as first through fourth sections of oxidation prevention cover film that are separated from each other and aligned directly above first through fourth mark portions in a pattern, as would be necessary to meet the features of claim 9. Applicant therefore respectfully submits that the semiconductor device of claim 9 distinguishes over the Sony reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 9, is improper for at least these reasons.

The semiconductor device of claim 16 includes in combination a substrate; an alignment mark "on the main surface of the substrate, wherein the alignment mark is strip-like and has a shape of a polygon without corners along a plane parallel to the main surface of the substrate"; and an oxidation prevention cover film "aligned directly above the alignment mark, wherein the oxidation prevention cover film is a closed-loop strip and has the shape of the polygon". Applicant respectfully submits that the prior art as relied upon does not disclose these features.

Particularly, silicon dioxide layer 15 and photoresist layer 16 in Fig. 4 of the Sony reference are planar and formed over an entirety of the surface of the structure as illustrated, and thus cannot be interpreted as an oxidation prevention cover film that is a closed-loop strip and that has the shape of a polygon, as would be necessary to meet the features of claim 16. Applicant therefore respectfully submits that the semiconductor device of claim 16 distinguishes over the Sony reference as relied upon

by the Examiner, and that this rejection, insofar as it may pertain to claims 16-18, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 3, 7, 8, 10, 14, 15, 19, 20 and 22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sony reference. Applicant respectfully submits that the Sony reference as herein relied upon does not overcome the above noted deficiencies as set forth above with respect to claims 1, 9 and 16, and that this rejection, insofar as it may pertain to the above noted claims, is improper for at least these reasons.

Claims 4, 11 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sony reference in view of the Sato et al. reference (Japanese Patent Publication No. 2002-64055). Applicant respectfully submits that the Sato et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon prior art, and that this rejection is therefore improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

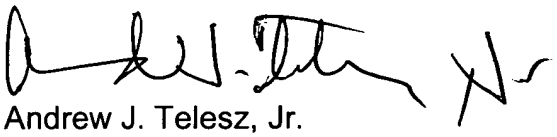
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.117, 1.136(a) and 41.37(e), the Applicant hereby petitions for an extension of one (1) month to November 30, 2006, for the period in which to file responsive to the Notice of Appeal. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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